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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,468	11/07/2001	Shinichi Shimomaki	01727/LH	2858

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EXAMINER	
JORGENSEN, LELAND R	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,468	SHIMOMAKI, SHINICHI	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 – 8 and 12 - 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al., USPN 5,490,000.

Claims 1 and 12

Tanaka teaches a liquid crystal display device comprising a liquid crystal display panel having a plurality of signal lines [data lines (graduation serial lines) 6], a plurality of scanning lines [gate lines (scanning lines) 5], and a plurality of display pixels arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements [TFTs 4]. Tanaka, col. 6, lines 2 – 43; and figure 2. A driver which supplies [though column driver 22] the plurality of signal lines with a display signal in a field period, and which supplies [through row driver 21] the plurality of scanning lines with a scanning signal, to apply the display signal to the plurality of display pixels. Tanaka, col. 6, lines 29 – 37; col. 41 – 43; and figures 2 and 4.

The driver includes means which supplies a predetermined initialization signal voltage [first reset pulse P12 and second reset pulse P13 shown in FIG. 12H] to the signal line [data line 6] and supplies a first gate pulse [pulse applied to gate lines of first row during first half selection period of period of pixels of first to eighth rows shown in FIG. 12A] as the scanning signal to the scanning line [gate line 5], thereby applying the initialization signal to the display pixel, and

thereafter supplies the display signal [write pulse P14] to the signal lines and supplies a second gate pulse [pulse applied to gate lines of first row during second half selection period of period of pixels of first to eighth rows shown in FIG. 12A] as the scanning signal to the scanning line, thereby applying the display signal to the display pixel, at least one signal application period set within the field period [one frame]. Tanaka, col. 15, lines 25 – col. 16, line 65; and figures 12A – 12H.

Claim 2

Tanaka teaches that the display panel includes a plurality of the pixel electrodes arrayed in a matrix through the elements, and common electrodes [counter electrode 7] opposed to the pixel electrodes, and the display pixels comprise the pixel electrodes, the common electrodes, and liquid crystal sandwiched between the pixel electrodes and the common electrodes. Tanaka, col. 6, lines 2 – 42; and figures 1 & 2.

Claim 3

Tanaka teaches that each of the switching elements of the liquid crystal display panel includes a thin film transistor. Tanaka, col. 6, lines 16 – 17.

Claims 4 and 13

Tanaka teaches that the driver applies the initialization signal voltage to the display pixels and thereafter applies the display signal after a predetermined hold time, in the signal application period in the field period, and the hold time is set to a time equal to or longer than a voltage-write response time of the display pixels. Tanaka, col. 15, lines 25 – col. 16, line 65; and figures 12A – 12H.

Claims 5 and 14

Tanaka teaches that the initialization signal voltage in the driver has a value equal to or higher than a maximum voltage value of the display signal. Tanaka, figure 12H.

Claims 6 and 15

Tanaka teaches that the driver applies the initialization signal voltage and the display signal to the display pixels connected to the scanning lines of the liquid crystal display panel, at a predetermined time interval, sequentially for every one of the scanning lines, in the signal application period in the field period, and the time interval is set to a value at which timings of applying the initialization signal voltage and the display signal to every one of the display pixels connected to each of the scanning lines do not overlap with each other. Tanaka, col. 15, lines 25 – col. 16, line 65; and figures 12A – 12H.

Claims 7 and 16

Tanaka teaches that application timing is set such that the driver applies the initialization signal voltage simultaneously to all of the display pixels of the liquid crystal display panel, and thereafter applies the display signal to the display pixels connected to the scanning lines of the liquid crystal display panel, at a predetermined time interval, sequentially for every one of the scanning lines in the signal application period in the field period. Tanaka, col. 15, lines 25 – col. 16, line 65; and figures 12A – 12H.

Claims 8 and 17

Tanaka teaches that the driver provides three signal application periods [second half selection of period of pixels in first row, second row, and third row] in one field period. Tanaka, col. 15, lines 25 – col. 16, line 65; and figures 12A – 12C.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 9 – 11, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al., in view of Taira et al., USPN 6,825,823 B1.

Claims 9 – 11, 18, and 19

Tanaka does not specifically teaches that the display signal comprises first, second, and third color component signals.

Taira teaches that the display signal comprises first, second, and third color component signals. Taira, col. 3, lines 21 – 24; and figures 8 – 10.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the first, second, and third color component signals as taught by Taira with the device and method as taught by Tanaka to provide that the driver applies the initialization signal voltage and thereafter applies any one of the first, second, and third color component signals, to the display pixels connected to the scanning lines of the liquid crystal display panel, sequentially for every one of the scanning lines in each of the signal application periods of the field period. This would allow a color display.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mizukata et al., USPN 5,598,177; Tanaka, USPN 5,895,108; Moon, USPN 5,825,343; and Kusafuka et al., USPN 5,995,074 (cited in prior action), each teach a two gate pulses per period.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 703-305-2650 (or 571-272-7768 after March 2005). The examiner can normally be reached on Monday through Friday, 10:00 a.m. through 6:00 p.m..

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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DENNIS-DOON CHOW
PRIMARY EXAMINER